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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/522,428	03/09/2000	Shunpei Yamazaki	SEL-165	3238

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EXAMINER	
PATEL, NITIN	

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 08/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

SUPPLEMENTAL **Notice of Allowability**	**Application No.** 09/522,428	**Applicant(s)** YAMAZAKI ET AL.	
	Examiner Nitin Patel	**Art Unit** 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *5/19/2006*.

2. ☒ The allowed claim(s) is/are *3-8,20-25,27-32,34-39,41-46,48-53,55-60,62-67,69-74,77-82,84-88,91-96,99-104,107-112,115-120,123-128,131-136,139-144,147-153 Now renumbered 1-114 respectively*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Nitin Patel

Nitin Patel
Examiner
Art Unit: 2629

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mark Murphy (registration No. 34,225) on 03/17/2006.

3. The application has been amended as follows:

I). **Claim 3 has been replaced with following amended claim 3.**

a). A display device comprising:

a plurality of pixels disposed in matrix over a substrate;

an active matrix circuit comprising a plurality of pixels TFT over said substrate, each of said pixel comprising at least first and second thin film transistors and a pixel electrode wherein a gate electrode of the first thin film transistor is electrically connected to a gate line and a gate electrode of the second thin film transistor is electrically connected to a drain region of the film thin transistor, and the pixel electrode is electrically connected to one of source and drain regions of the second thin film transistor;

a source driver and a gate driver which drive said active matrix circuit over said substrate; and

a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides said n bit digital video data to said source driver, where

said m and said n are integers equal to or larger than 2 and satisfy m>n, wherein said circuit is formed over substrate;

wherein each step of a voltage level for said voltage gray scale method is designated as (VH-VL)2n, where VH is the highest voltage level of voltages inputted to DA converter circuit, and VL is the lowest level of voltage inputted to said D/A converter circuit.

II). **Claim 4 has been replaced with following amended claim 4.**

a). A display device comprising:

a plurality of pixels disposed in matrix over a substrate;

an active matrix circuit comprising a plurality of pixels TFT over said substrate,

a source driver and a gate driver which drive said active matrix circuit over said substrate; and

a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides said n bit digital video data to said source driver, where said m and said n are integers equal to or larger than 2 and satisfy m>n, wherein said circuit is formed over substrate;

wherein each step of a voltage level for said voltage gray scale method is designated as (VH-VL)2n, where VH is the highest voltage level of voltages inputted to DA converter circuit, and VL is the lowest level of voltage inputted to said D/A converter circuit, and

wherein one frame period comprises 2 to the m-n subframe periods.

III). **Claim 5 has been replaced with following amended claim 5.**

a). A display device comprising:

a plurality of pixels disposed in matrix over a substrate;

an active matrix circuit comprising a plurality of pixels TFT over said substrate, each of said pixel comprising at least first and second thin film transistors and a pixel electrode wherein a gate electrode of the first thin film transistor is electrically connected to a gate line and a gate electrode of the second thin film transistor is electrically connected to a drain region of the film thin transistor, and the pixel electrode is electrically connected to one of source and drain regions of the second thin film transistor;

a source driver and a gate driver which drive said active matrix circuit over said active matrix circuit,

wherein n bit information out of m bit digital video data inputted from an external is used for a voltage gray scale method and (m-n) bit information is used for a time ration gray scale method, where said m and n are integers equal to or larger than 2 and satisfy m>n,

wherein each step of a voltage level for said voltage gray scale method is designated as (VH-VL)2n, where VH is the highest voltage level of voltages inputted to DA converter circuit, and VL is the lowest level of voltage inputted to said D/A converter circuit, and

wherein an image displayed by an image gray scale of (2 to the m- ((2 to the m-n)-1) patterns.

IV). **Claim 6 has been replaced with following amended claim 6.**

a). A display device comprising:

a plurality of pixels disposed in matrix over a substrate;

an active matrix circuit comprising a plurality of pixels TFT over said substrate,

a source driver and a gate driver which drive said active matrix circuit,

wherein n bit information out of m bit digital video data inputted from an external is used for a voltage gray scale method and (m-n) bit information is used for a time ratio gray scale method, where said m and n are integers equal to or larger than 2 and satisfy m>n,

wherein each step of a voltage level for said voltage gray scale method is designated as (VH-VL)2n, where VH is the highest voltage level of voltages inputted to DA converter circuit, and VL is the lowest level of voltage inputted to said D/A converter circuit and

wherein one frame period comprises 2 to the m-n subframe periods, and

wherein an image is displayed by an image gray scale of (2 to the m- ((2 to the m-n)-1) patterns.

V). **Claim 7 has been replaced with following amended claim 7.**

a). A display device comprising:

a plurality of pixels disposed in matrix over a substrate;

an active matrix circuit comprising a plurality of pixels TFT over said substrate, each of said pixel comprising at least first and second thin film transistors and a pixel electrode wherein a gate electrode of the first thin film transistor is electrically connected to a gate line and a gate electrode of the second thin film transistor is electrically

connected to a drain region of the film thin transistor, and the pixel electrode is electrically connected to one of source and drain regions of the second thin film transistor;

a source driver and a gate driver which drive said active matrix circuit over said substrate; and

a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides said n bit digital video data to said source driver, where said m and said n are integers equal to or larger than 2 and satisfy m>n, wherein said circuit is formed over substrate;

wherein each step of a voltage level for said voltage gray scale method is designated as (VH-VL) 2n, where VH is the highest voltage level of voltages inputted to DA converter circuit, and VL is the lowest level of voltage inputted to said D/A converter circuit, and

wherein an image is displayed by and image gray scale of (2 to the m-((2 to the m-n)-1) patterns.

VI). **Claim 8 has been replaced with following amended claim 8.**

a). A display device comprising:

a plurality of pixels disposed in matrix over a substrate;

an active matrix circuit comprising a plurality of pixels TFT over said substrate,

a source driver and a gate driver which drive said active matrix circuit over said substrate; and

a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides said n bit digital video data to said source driver, where said m and said n are integers equal to or larger than 2 and satisfy m>n, wherein said circuit is formed over substrate;

wherein each step of a voltage level for said voltage gray scale method is designated as (VH-VL)2n, where VH is the highest voltage level of voltages inputted to DA converter circuit, and VL is the lowest level of voltage inputted to said D/A converter circuit, and

wherein one frame period comprises 2 to the m-n subframe periods and

wherein an image is displayed by an image gray scale of (2 to the m-((2 to the m-n)-1) patterns.

REASON FOR ALLOWANCE

4. Claims 3-8,20-25,27-32,34-39,41-46,48-53,55-60,62-67,69-74,77-82,84-88,91-96,99-104,107-112,115-120,123-128,131-136,139-144,147-155 is allowed. Claims 1-2,9-19,26,33,40,47,54,61,68,75-76,83,89-90,97-98,105-106,113-114,121-122,129-130,137-138,145-146 has been cancelled.

5. The following is an examiner's statement of reason for allowance:

The prior art fails to teach or suggest a display device comprising:

a plurality of pixels disposed in matrix over a substrate;an active matrix circuit comprising a plurality of pixels TFT over said substrate, each of said pixel comprising at least first and second thin film transistors and a pixel electrode wherein a gate electrode of the first thin film transistor is electrically connected to a gate line and a gate electrode

of the second thin film transistor is electrically connected to a drain region of the film thin transistor, and the pixel electrode is electrically connected to one of source and drain regions of the second thin film transistor;a source driver and a gate driver which drive said active matrix circuit over said substrate; and a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides said n bit digital video data to said source driver, where said m and said n are integers equal to or larger than 2 and satisfy m>n, wherein said circuit is formed over substrate; wherein each step of a voltage level for said voltage gray scale method is designated as (VH-VL)2n, where VH is the highest voltage level of voltages inputted to DA converter circuit, and VL is the lowest level of voltage inputted to said D/A converter circuit as claimed in claim 3.

The prior art fails to teach or suggest a display device comprising:

a plurality of pixels disposed in matrix over a substrate; an active matrix circuit comprising a plurality of pixels TFT over said substrate, a source driver and a gate driver which drive said active matrix circuit over said substrate; and a circuit which converts m bit digital video data inputted from an external into n bit digital video data and provides said n bit digital video data to said source driver, where said m and said n are integers equal to or larger than 2 and satisfy m>n, wherein said circuit is formed over substrate; wherein each step of a voltage level for said voltage gray scale method is designated as (VH-VL)2n, where VH is the highest voltage level of voltages inputted to DA converter circuit, and VL is the lowest level of voltage inputted to said D/A

converter circuit, and wherein one frame period comprises 2 to the m-n subframe periods as claimed in claim 4.

The prior art fails to teach or suggest a display device comprising:

a plurality of pixels disposed in matrix over a substrate; an active matrix circuit comprising a plurality of pixels TFT over said substrate, each of said pixel comprising at least first and second thin film transistors and a pixel electrode wherein a gate electrode of the first thin film transistor is electrically connected to a gate line and a gate electrode of the second thin film transistor is electrically connected to a drain region of the film thin transistor, and the pixel electrode is electrically connected to one of source and drain regions of the second thin film transistor; a source driver and a gate driver which drive said active matrix circuit over said active matrix circuit, wherein n bit information out of m bit digital video data inputted from an external is used for a voltage gray scale method and (m-n) bit information is used for a time ration gray scale method, where said m and n are integers equal to or larger than 2 and satisfy m>n, wherein each step of a voltage level for said voltage gray scale method is designated as (VH-VL)2n, where VH is the highest voltage level of voltages inputted to DA converter circuit, and VL is the lowest level of voltage inputted to said D/A converter circuit, and wherein an image displayed by an image gray scale of (2 to the m-((2 to the m-n)-1) patterns as claimed in claims 5-8.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H. Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP Nitin Patel

March 19, 2006